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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Warren M. Farnworth

Serial No.: 10/043,362

Filed: January 9, 2002

For: STEREOLITHOGRAPHIC
METHODS FOR FABRICATING
HERMETIC SEMICONDUCTOR DEVICE
PACKAGES AND SEMICONDUCTOR
DEVICES INCLUDING
STEREOLITHOGRAPHICALLY
FABRICATED HERMETIC PACKAGES

Examiner: D. Zarneke

Group Art Unit: 2827

Attorney Docket No.: 2269-4212.1US
(99-0306.01/US)

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SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In compliance with the duty to disclose information material to patentability pursuant to 37 C.F.R. § 1.56, it is respectfully requested that this Supplemental Information Disclosure Statement be entered and the documents listed on attached Form PTO-1449 or PTO/SB/08 be considered by the Examiner and made of record. Copies of the listed documents are enclosed pursuant to 37 C.F.R. § 1.98(a).

In accordance with 37 C.F.R. § 1.97(g) and (h), filing of this Supplemental Information Disclosure Statement is not to be construed as a representation that a search has been made or an admission that the information cited herein is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b). Further, no representation is made by Applicant herein that no other possible material information as defined in 37 C.F.R. § 1.56 (b) exists.



Serial No. 10/043,362

U.S. Patent Documents

<u>U.S. Patent No.</u>	<u>Publication Date</u>	<u>Patentee</u>
4,769,345	09/06/88	Butt et al.
4,821,151	04/11/89	Pryor et al.
4,866,571	09/12/89	Butt
4,967,260	10/30/90	Butt
5,014,159	05/07/91	Butt
5,323,051	06/21/94	Adams et al.
6,251,488	06/26/01	Miller et al.
6,259,962	07/10/01	Gothait
6,268,584	07/31/01	Keicher et al.
6,337,122	01/08/02	Grigg et al.
6,391,251	05/21/02	Keicher et al.
6,482,576	11/19/02	Farnworth et al.
6,489,007	12/03/02	Grigg et al.
6,524,346	02/25/03	Farnworth
6,544,821	04/08/03	Akram
6,544,902	04/08/03	Farnworth
6,549,821	04/15/03	Farnworth et al.
6,562,278	05/13/03	Farnworth et al.
6,585,927	07/01/03	Grigg et al.
6,635,333	10/21/03	Grigg et al.

Other Documents

U.S. Patent Application Publication No. 2002/0098623 A1 to Akram, dated July 25, 2002

U.S. Patent Application Publication No. 2002/0171177 A1 to Kritchman et al., dated November 21, 2002

U.S. Patent Application Publication No. 2003/0003180 A1 to Farnworth et al., dated January 2, 2003

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U.S. Patent Application Publication No. 2003/0043360 A1 to Farnworth., dated March 6, 2003

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U.S. Patent Application Publication No. 2003/0092220 A1 to Akram, dated May 15, 2003

U.S. Patent Application Publication No. 2003/0093173 A1 to Farnworth et al., dated May 15, 2003

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U.S. Patent Application Publication No. 2003/0151167 A1 to Kritchman et al., dated August 14, 2003

U.S. Patent Application Publication No. 2003/0201531 A1 to Farnworth et al., dated October 30, 2003

U.S. Patent Application Publication No. 2003/0203158 A1 to Farnworth et al., dated October 30, 2003

U.S. Patent Application Publication No. 2003/0207213 A1 to Farnworth, dated November 6, 2003

MILLER et al., "Maskless Mesoscale Materials Deposition", Deposition Technology, September 2001, pages 20-22

MILLER, "New Laser-Directed Deposition Technology", Microelectronic Fabrication, August 2001, page 16

Webpage, Objet Prototyping the Future, Objet FullCure700 Series, 1 page

Webpage, Objet Prototyping the Future, How it Works, 2 pages

U.S. Patent Application No. 09/589,841, filed June 8, 2000, entitled "Stereolithographic Methods for Forming a Protective Layer on a Semiconductor Device Substrate and Substrates Including Protective Layers So Formed", inventor Farnworth et al.

U.S. Patent Application No. 09/651,930, filed August 31, 2000, entitled "Semiconductor Device Including Leads in Communication with Contact Pads Thereof and a Stereolithographically Fabricated Package Substantially Encapsulating the Leads and Methods for Fabricating the Same", inventor Salman Akram

U.S. Patent Application No. 10/370,755, filed February 20, 2003, entitled "Chip Scale Package Structures and Method of Forming Conductive Bumps Thereon", inventor Warren M. Farnworth

U.S. Patent Application No. 10/608,749, filed June 26, 2003, entitled "Methods for Labeling Semiconductor Device Components", inventor Grigg et al.

U.S. Patent Application No. 10/672,098, filed September 26, 2003, entitled "Apparatus and Methods for Use in Stereolithographic Processing of Components and Assemblies", inventor Warren M. Farnworth

U.S. Patent Application No. 10/690,417, filed October 20, 2003, entitled "Methods of Coating and Singulating Wafers and Chip-Scale Packages Formed Therefrom", inventor Farnworth et al.

Applicant offers to supply any explanation or discussion of the documents which the Examiner feels is necessary or desirable and which is requested.

Serial No. 10/043,362

This Supplemental Information Disclosure Statement is believed to be filed before the mailing date of the first Office Action on the merits and concurrently with the filing of an RCE in the above-identified application.

Respectfully submitted,

A handwritten signature in black ink, appearing to read "Brick G. Power", with a long horizontal flourish extending to the right.

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Date: November 25, 2003
BGP/sls:djp

Enclosures: Form PTO-1449 or PTO/SB/08
Copy of documents cited

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet	1	of	4
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Complete if Known

Application Number	10/043,362
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Filing Date	January 9, 2002
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First Named Inventor	Warren M. Farnworth
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Group Art Unit	2827
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Examiner Name	D. Zarneke
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Attorney Docket Number	4212.1 US (99-0306.01/US)
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U.S. PATENT DOCUMENTS

Examiner Initials *	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code ² (if known)			
		US-4,769,345	09/06/88	Butt et al.	
		US-4,821,151	04/11/89	Pryor et al.	
		US-4,866,571	09/12/89	Butt	
		US-4,967,260	10/30/90	Butt	
		US-5,014,159	05/07/91	Butt	
		US-5,323,051	06/21/94	Adams et al.	
		US-6,251,488	06/26/01	Miller et al.	
		US- 6,259,962	07/10/01	Gothait	
		US- 6,268,584	07/31/01	Keicher et al.	
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		US- 6,391,251	05/21/02	Keicher et al.	
		US- 6,482,576	11/19/02	Famworth et al.	
		US- 6,489,007	12/03/02	Grigg et al.	
		US- 6,524,346	02/25/03	Famworth	
		US- 6,544,821	04/08/03	Akram	
		US- 6,544,902	04/08/03	Famworth	
		US- 6,549,821	04/15/03	Famworth et al.	
		US- 6,562,278	05/13/03	Famworth et al.	
		US- 6,585,927	07/01/03	Grigg et al.	
		US- 6,635,333	10/21/03	Grigg et al.	

FOREIGN PATENT DOCUMENTS

[illegible]

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¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

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Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i> Sheet <u>2</u> of <u>4</u>	Complete if Known	
	Application Number	10/043,362
	Filing Date	January 9, 2002
	First Named Inventor	Warren M. Farnworth
	Group Art Unit	2827
	Examiner Name	D. Zarneke
	Attorney Docket Number	4212 IUS (99-0306 01/IUS)

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		U.S. Patent Application Publication No. 2002/0098623 A1 to Akram, dated July 25, 2002	
		U.S. Patent Application Publication No. 2002/0171177 A1 to Kritchman et al., dated November 21, 2002	
		U.S. Patent Application Publication No. 2003/0003180 A1 to Farnworth et al., dated January 2, 2003	
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Examiner Signature		Date Considered	
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**INFORMATION DISCLOSURE
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Sheet 3 of 4

Complete if Known

Application Number	10/043,362
Filing Date	January 9, 2002
First Named Inventor	Warren M. Farnworth
Group Art Unit	2827
Examiner Name	D. Zarneke
Attorney Docket Number	4212-11JS (99-0306-01/1JS)

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		U.S. Patent Application Publication No. 2003/0093173 A1 to Farnworth et al., dated May 15, 2003	
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		U.S. Patent Application Publication No. 2003/0207213 A1 to Farnworth, dated November 6, 2003	
		MILLER et al., "Maskless Mesoscale Materials Deposition", Deposition Technology, September 2001, pages 20-22	
		MILLER, "New Laser-Directed Deposition Technology", Microelectronic Fabrication, August 2001, page 16	
		Webpage, Objet Prototyping the Future, Objet FullCure700 Series, 1 page	
		Webpage, Objet Prototyping the Future, How it Works, 2 pages	
		U.S. Patent Application No. 09/589,841, filed June 8, 2000, entitled "Stereolithographic Methods for Forming a Protective Layer on a Semiconductor Device Substrate and Substrates Including Protective Layers So-Formed", inventor Farnworth et al.	

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		Filing Date	January 9, 2002
		First Named Inventor	Warren M. Farnworth
		Group Art Unit	2827
		Examiner Name	D. Zarneke
		Attorney Docket Number	4212-111S (99-0306 01/US)

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		U.S. Patent Application No. 10/370,755, filed February 20, 2003, entitled "Chip Scale Package Structures and Method of Forming Conductive Bumps Thereon", inventor Warren M. Farnworth	
		U.S. Patent Application No. 10/608,749, filed June 26, 2003, entitled "Methods for Labeling Semiconductor Device Components", inventor Grigg et al.	
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